

Muon Time-of-Passage Estimation for Standalone MDT Trigger

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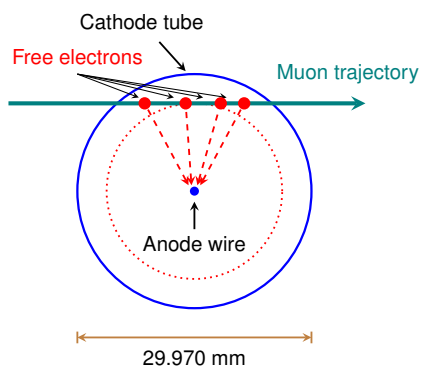


Motivation & Context

- **HL-LHC Upgrade at CERN:** The High-Luminosity Large Hadron Collider will bring up to 10x higher collision rates.
- **ATLAS Experiment at HL-LHC:** Tracking muons is vital for discovering new physics phenomena.
- **Trigger System:** Real-time filtering to keep only the significant collision events. The aging hardware muon trigger will be overwhelmed.
- **Novel Approach:** Utilize newly available Monitored Drift Tube (MDT) data to design a robust, **standalone MDT trigger** pipeline.

The Hardware Bottleneck

- **MDT Latency:** Gas-filled drift tubes track passing muons via electron drift (up to 720 ns latency).
- **Inference Budget:** The algorithm must predict the time of the muon's closest approach in under 1 μ s.
- **Hardware Limits:** Inference must run exclusively on FPGAs.
- **Background Noise:** Retain prediction robustness under severe background noise rates of the HL-LHC.



MDT cross-section and electron drift toward the central wire.

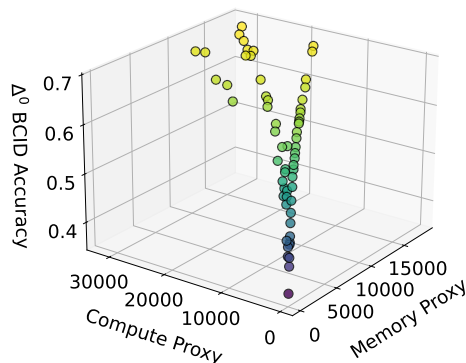
The Proposed Architecture

Line Graph Neural Network (LGNN)

The Solution: Developed a custom, novel architecture based on Graph Neural Networks. A custom paired graph representation allows for efficient event representation while eliminating explicit edge features:

- Message-passing achieved exclusively via **matrix multiplication**.
- Strict **static memory footprint**.
- Model retains high accuracy and enables **FPGA implementation**.

Hardware-Aware Optimization

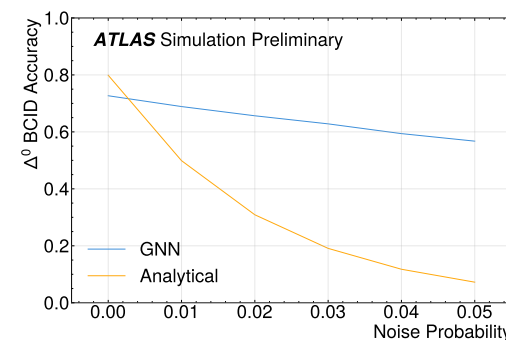


3D Pareto front mapping hardware constraints.

- **NSGA-II Algorithm:** Multi-objective genetic optimization to balance hardware utilization and model accuracy.
- **The Result:** A large set of solutions optimal for each combination of predictive accuracy, memory, and latency costs.

Noise Robustness

- **Baseline Failure:** Analytical baseline solutions perform well in clean data but degrade rapidly under increasing noise levels.
- **LGNN Resilience:** Zero-shot and fine-tuned LGNN architectures maintain robustness, while retaining hardware implementability.



Superior noise robustness of the LGNN approach compared to baselines.

Key Contributions

- **Trigger Viability:** Proved machine learning is a feasible, high-performance solution for the MDT trigger.
- **Hardware Readiness:** Designed a novel FPGA-ready LGNN architecture.
- **Resilient Performance:** Delivered state-of-the-art accuracy that massively outperforms geometric baselines under severe background noise.
- **Future Impact:** Establishes a robust foundation for ongoing research into efficient FPGA implementations of LGNNs.
- Results were showcased across numerous presentations at CERN, prominently featured in the *All Hands Next Generation Triggers 2026* sessions.