Digital I2C/APB block using low-power techniques

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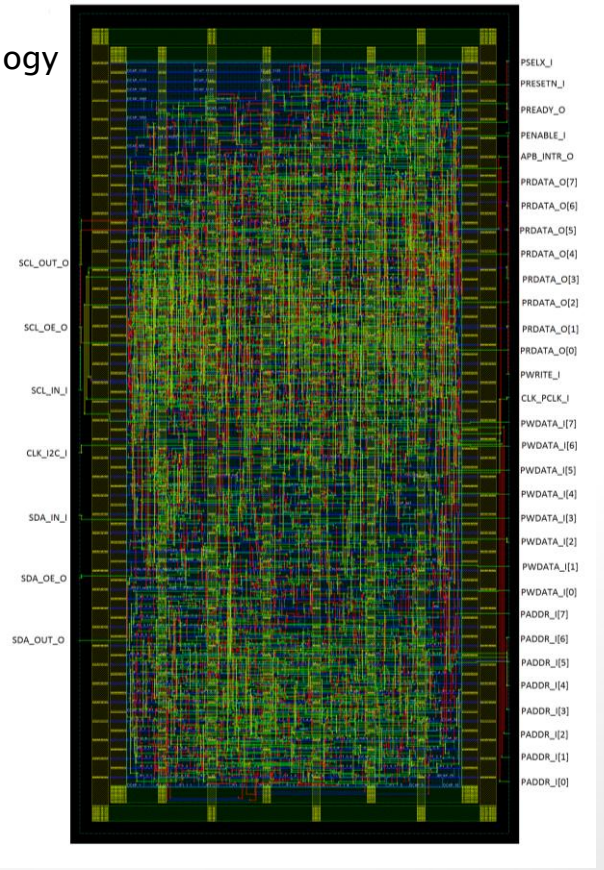
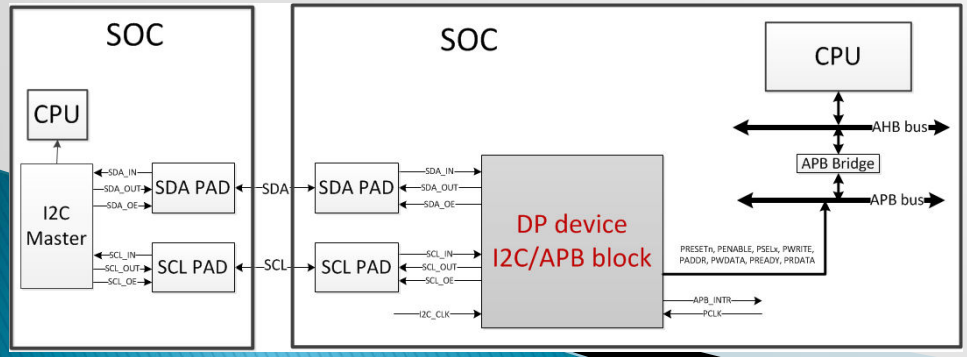


Low power – aware design has become a very important part of designing today's chips. The goal of this thesis was to design a I2C slave interface device that is integrated into a SOC that is connected to APB bus. Low power techniques were designed during the design. Results of several different techniques are compared.

Use of the block:
- Communication between Systems on Chip (SOCs)
- Connection of an ASIC to I2C Master (that can be another SoC or also a micro-controller)

Parts of the Masters thesis:
- Comparing Low-power techniques
- RTL design in Verilog 2001
- Verification including FSM coverage and code-coverage
- Use of low-power techniques – lowest frequency possible and clock gating
- Physical design and power consumption evaluation in 65nm technology

Result:
- Digital hard-macro



Power savings achievements:

Compared with the case without any low-power techniques use

Consumption mode	Clock gating type		
	AUTO	MAN	MAN-AUTO
IDLE	39.16%	63.21%	64.24%
COMMUNICATION	40.37%	-6.90%	37.07%