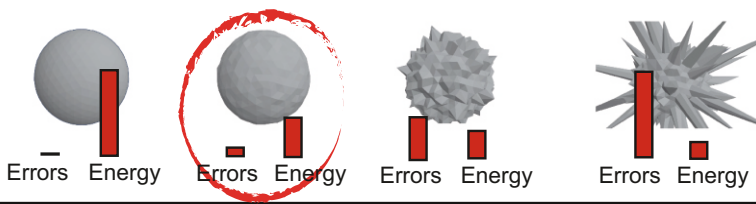


Towards Energy-Efficient System Design

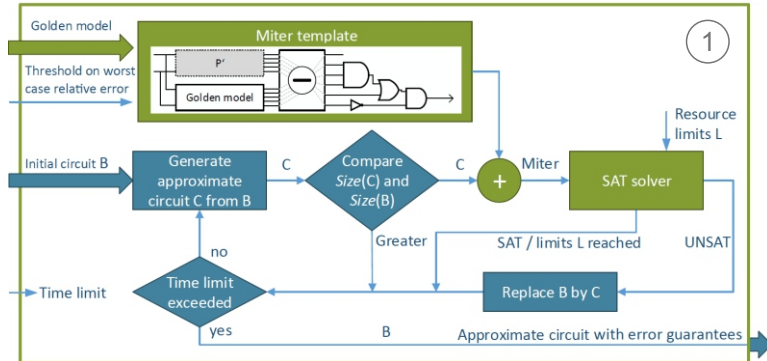
Problem

- The reduction of energy consumption of electronic devices has become one of the greatest challenges in the computer industry.
- **Approximate computing** is a new and promising research field that aims at reducing system resource demands by relaxing the requirement that its underlying operations are always performed correctly. Chippa et al. (DAC 2013) claims that almost 80 % of runtime is spent in procedures that could be approximated.
- We propose to use the **advanced formal verification** methods to speed up the design process and provide formal guarantees on the approximation error.
- **Example:** different designs of a sphere with various trade-offs between error and power consumption.

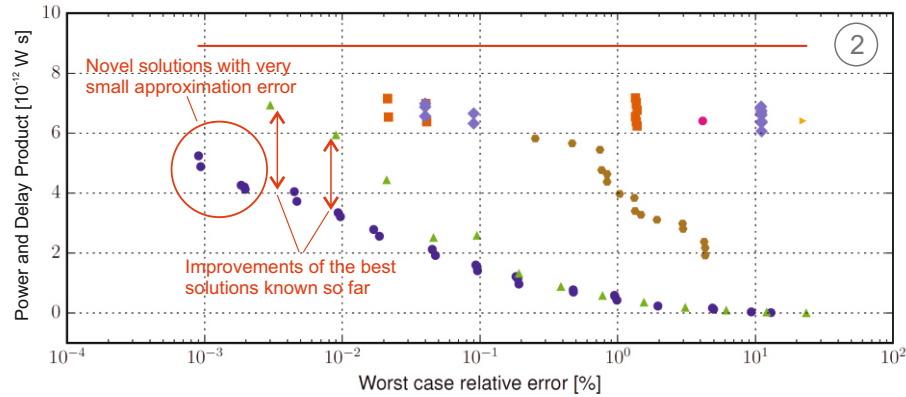


Contribution

- The newly designed method integrates formal verification methods (namely SAT solving) into a circuit optimisation algorithm based on Cartesian Genetic Programming (CGP).
- To ensure scalability with respect to the complexity of the circuit, we developed a novel search strategy that drives the evolutionary algorithm towards promptly verifiable solutions (demonstrated in plot (1)).
- The method was integrated into the state-of-the-art hardware synthesis tool ABC.
- Using our approach we synthesised high-quality Pareto fronts of approximate 32-bit multipliers and 128-bit adders. The fronts provide various trade-offs between the error and the on-chip area directly affecting the energy consumption. Such results have never been published before as current methods struggle to approximate larger than 12/16-bit multipliers/adders when formal guarantees are required.
- The results of this work were published in Ceska et al. (ICCAD 2017) on a rank A international conference.

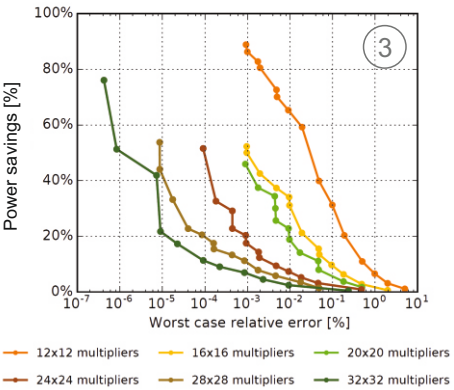


Experiments and Results



- Proposed method
- M1Lit (ConfMult16x16Lit)
- M1V1 (ConfMult16x16V1)
- M2 (BSDLC)
- M3 (Bit-width reduction)
- M4 (Kulkarni 2x2)
- M5 (EvoApproxLib8)
- Accurate (*)

- We performed an extensive experimental evaluation on multipliers and adders of various bit width (up to 32 and 128 bits respectively) and different approximation errors. The most significant results are demonstrated in the included plots.
- In plot (2), we show the comparison of our 16-bit multiplier approximations to other approximations (designed without formal guarantees) available in literature.
- Plot (3) shows estimated power savings for multipliers of various bit-widths against their worst-case relative error. 100% refers to the corresponding power of the accurate multiplier for a given bit width.



Current and Future Work

- The project continues as the PhD theme of the author and focuses on:
- more complex and problem-oriented error metrics,
 - understanding how the structure of the approximate circuits affects their verifiability,
 - generalisation of the approach towards sequential circuits and software approximation,
 - deployment of the approximate systems in real-world energy-aware applications like low-power signal processing or machine learning on a chip.