Hardware Acceleration of Operating Systems (Real-Time Task Scheduling)

- Faster Task Scheduling
- Lower Overhead of the Operating System
- Higher CPU Utilization
- More Real-Time Tasks Meet Their Deadlines

2 Custom Instructions
- `task_schedule` – inserts a new task into the queue ordered according to the deadline
- `task_kill` – removes any existing task from the queue according to the ID of the task

Chip Area Costs

<table>
<thead>
<tr>
<th></th>
<th>control unit</th>
<th>per task</th>
<th>systolic array node</th>
<th>total*</th>
</tr>
</thead>
<tbody>
<tr>
<td>D-FF</td>
<td>1</td>
<td>log(N) + D_width</td>
<td>2 per_task + 2</td>
<td>957</td>
</tr>
<tr>
<td>MUX</td>
<td>1</td>
<td>3 log(N) + D_width</td>
<td>0</td>
<td>2401</td>
</tr>
<tr>
<td>NAND</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>NOR</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>32</td>
</tr>
<tr>
<td>AND</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>32</td>
</tr>
<tr>
<td>OR</td>
<td>D_width + 1</td>
<td>2</td>
<td>0</td>
<td>85</td>
</tr>
<tr>
<td>XOR</td>
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<td>log(N)</td>
<td>0</td>
<td>160</td>
</tr>
<tr>
<td>COMP</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>32</td>
</tr>
<tr>
<td>DEC</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>32</td>
</tr>
</tbody>
</table>

* - for N = 32, D_width = 5 and 4-stage pipelining

- Number of tasks in the system
- Bit width of the deadline times
- Bit width of the task ID

Serial Architecture – Pipelining

Parallel Architecture – Shift Registers

FPGA Synthesis Results

- Device Family: Altera Cyclone II
- Device: EP2C70F896C6
- Logic Elements: 4547 (7%)
- Combinational Functions: 3912 (6%)
- Dedicated Logic Registers: 957 (1%)
- Max. Number of Tasks: 32
- Deadline Accuracy: 20 bits (1 us)

Verification

- Pre-Layout Simulations
- Software Implemented Simulations (C Language Console Application)
- Functional BIST - synthesizable verification

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